Al Baumbaugh

Preliminary!!!

New BLM Theory of Operation

I) Basics

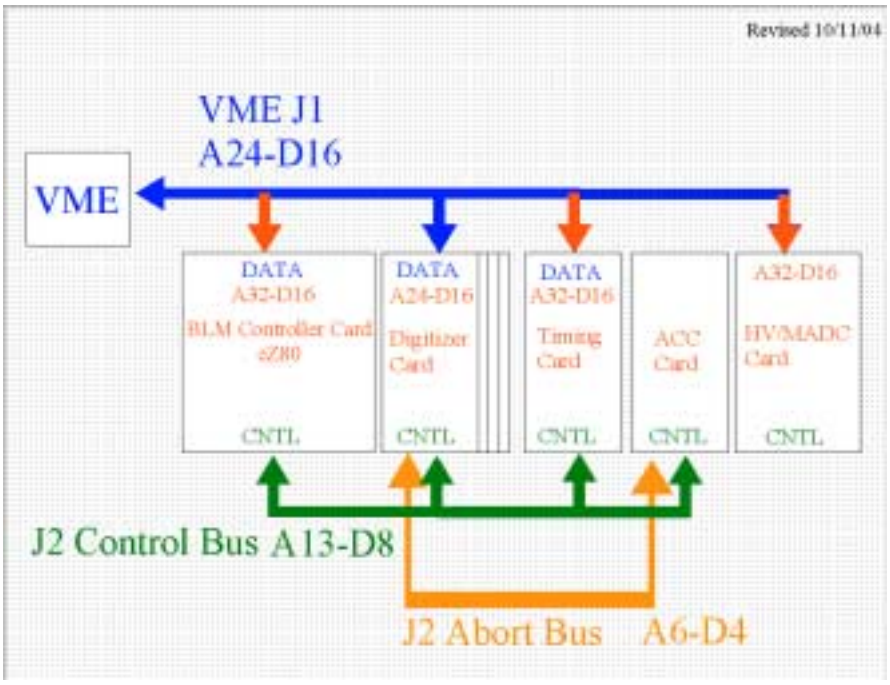
The primary goal of the new BLM system is to protect the Tevatron from damaging quenches caused by beam losses.

The Basic principle of operation of the new BLM system is to integrate for a short period of time (Typically 21 microseconds) and digitize to 16 bits. There are 2 integrators/channel, running in a "Ping-Pong" mode so that no loss is missed. One channel is integrating while the other is being digitized and reset, it is the reset time, which sets the lower limit of 12 microseconds.

Once the integrated loss is digitized, the data is used to construct several numbers that are compared against thresholds to generate abort signals. These constructed data are sliding sums, which are a measure of the integrated loss over a variety of time scales from a single reading (12 microseconds) to the integrated loss over a period of up to 1.4 seconds.

The Abort signal is made in hardware by looking at these sums and thresholds as well as the number of channels requesting an abort.

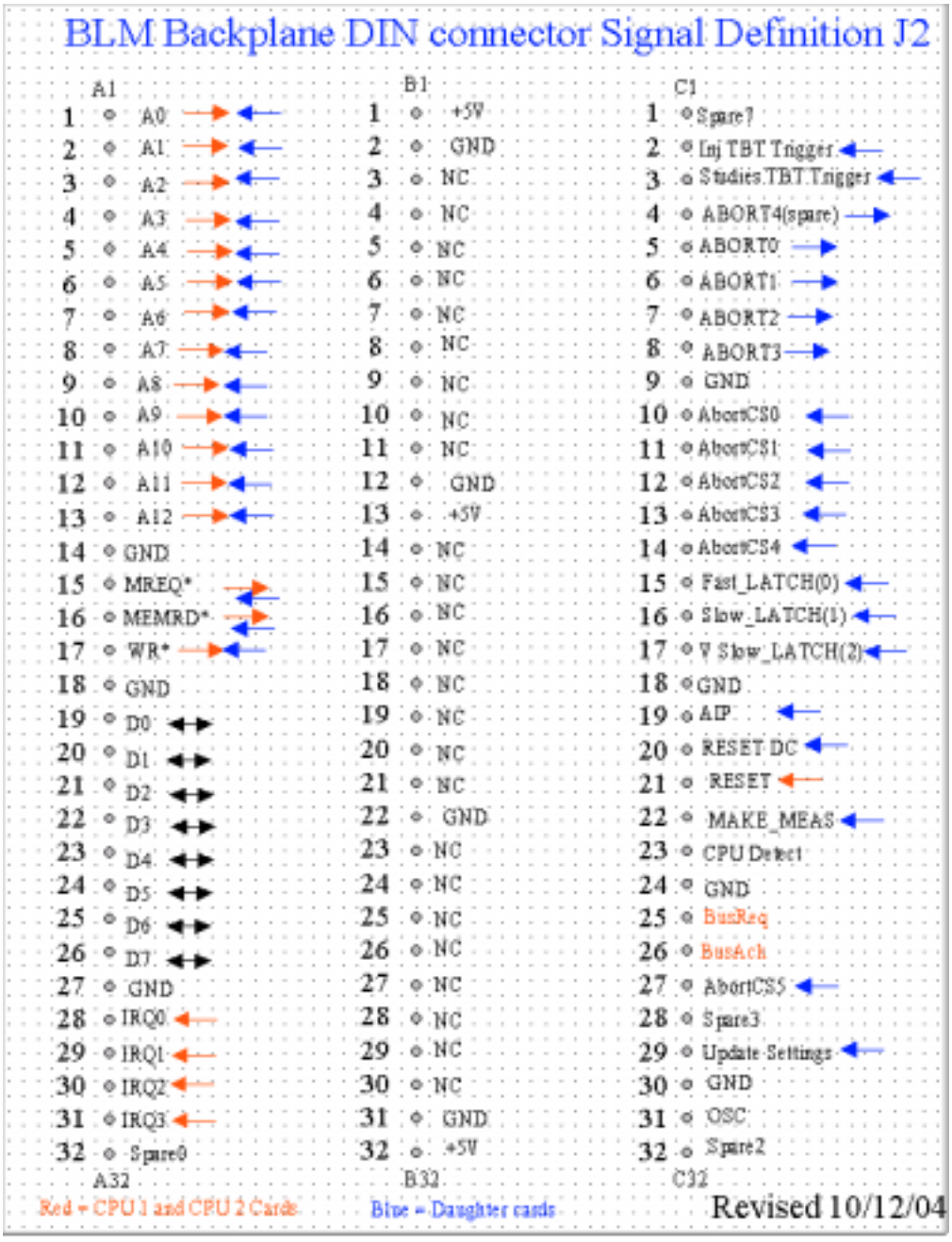
II) Implementation



The BLM system is implemented in 6U VME Crate and consists of 5 different types of cards. These are:

1) Digitizer Card
2) Clock and timing Card
3) Abort Controller Card
4) High Voltage Card
5) Controller Card

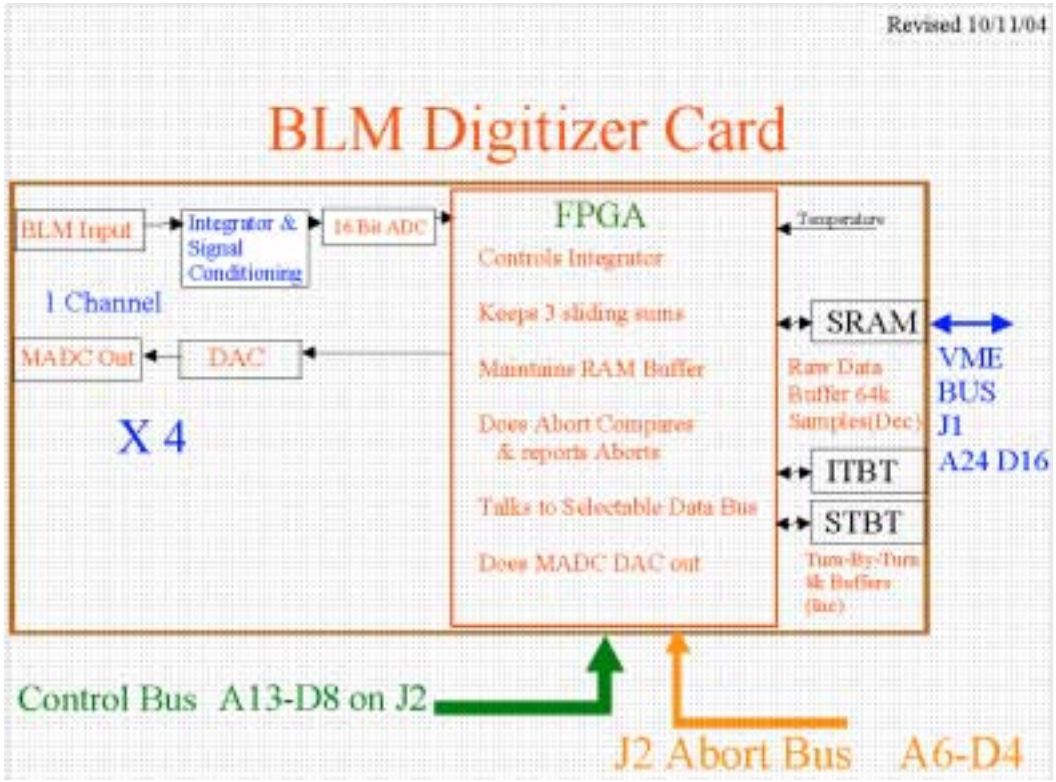
A Control Bus using the user-defined pins on the J2 VME connector handles all of the critical BLM controls. This buss has 13 address lines and 8 data lines, the Controller Card is the only master on this bus, and all other cards are slaves. These cards are described in the next section. Also on the J2 connector is the Abort Concentrator Bus, the ACC is the master and the digitizer cards are the slaves.



III) Digitizer Card

The digitizer card is the primary data collector in the system, it has on board

1) Control Bus Interface for setting parameters
2) 512 kbytes of RAM for storing Raw Measurements Data (RMD)
3) 128kbytes of RAM for storing 2 banks of 8k TBT data
4) 4 Loss monitor Channels, 4 dual integrators, 4 16-bit ADCs
5) 4 16-bit DACs for MADC outputs
6) a VME interface only used for reading RMD and only accessible when system is stopped, and for reading TBT data when TBT Not in operation.
7) A 4 bit switch selectable card number which sets channel numbers and both Control Bus and VME addresses. Note On Control Bus CA12=0 for digitizer cards. CA8:11=Switch for card select.
8) A state machine that runs the digitizer section and makes the 4 sliding sums for each channel. It also maintains the RMD RAM circular buffer.
9) An Abort channel select and 4 abort line drivers, these 4 lines are for:
   a) Immediate Loss Abort threshold (few microseconds)
   b) Fast Loss Abort Threshold (few milliseconds)
   c) Slow Loss Abort Threshold (few 10s of milliseconds)
   d) Very Slow Loss Abort Threshold (few seconds)



The operation of the digitizer card is controlled by signals on the control bus. These signals are:

1) Reset, Reset. This signal is the BLM Crate reset signal, driven by the Controller Card (CC) it should reset the state machine on the DC.
2) Reset_DC, Reset Digitizer Card. This signal clears the sliding sums and resets the RMD pointer to 0000. This signal typically is used to initialize the DC and get ready for data taking.
3) Make_meas, Make Measurement. This signal causes the DC to switch from A to B or B to A channels, latches the previous abort states, digitizes the reading, resets the integrator, calculates the sliding sums, and makes the abort

comparisons. This signal is generated on the Timing Card (TC) and typically runs continuously at about once every 20 microseconds. The sliding sums are made by adding the current reading to the sum and subtracting the oldest reading from the sum. The 3 sliding sums have 3 oldest data pointers, which point to the data in the RMD that is to be subtracted. There is also new data pointer, which sets the location in the RMD where the newest reading is stored. Once the sliding sums are calculated, the state machine might "pre-Fetch" the 3 oldest data readings that will need to be subtracted during the next cycle.

4) Fast_Latch, This is a signal produced on the TC which tells the state machine to latch the current Fast_Sum into a register so the controller can read it
5) Slow_Latch, This is a signal produced on the TC which tells the state machine to latch the current Slow_Sum into a register so the controller can read it
6) VSlow_Latch, This is a signal produced on the TC which tells the state machine to latch the current Very_Slow_Sum into a register so the controller can read it
7) Abort_CS(0:5), Abort Channel select. These signals come from the Abort Controller (ACC) and are used to poll all the channels to request abort demand conditions. The State machine compares Abort_CS(2:5) with address switches 0,1,2,3 to determine if the requested channel is on this board. Then Abort_CS(0:1) are channels 0,1,2,3 on board. When selected, each channels 4 abort lines are driven onto the buss's Abort(0:3) lines. A channel requesting an abort drives the corresponding line low.
8) Abort(0:3), Abort lines 0,1,2,3. These are driven by the DC to the ACC in order for the ACC to determine how many channels are requesting an abort for each of the 4 abort types.
9) CA(0:12), Control Bus Address lines. These are used to address control and data within the state machine. These are driven by the CC.
10) Cdata(0:7) Control Bus Data Lines. These are the data lines used to read and write data to and from the state machine.
11) MemRD*, Memory read. This indicates that the current Control Bus cycle is a read.
12) MemWR*, Memory write. This indicates that the current Control Bus cycle is a write.
13) WE*, Memory Write Enable. This is the write strobe for data, data should be latches on the rising edge of WE*
14) ITBT Trigger. This is the injection Turns trigger and causes the raw data to be written into the 8k ITBT buffer. Once the buffer is full or the system stops, this data is readable via VME.
15) STBT Trigger. This is the TBT studies trigger and causes the next 8k raw measurements data to be written into the STBT Buffer. Once the buffer is full or the system stops, this data is readable via VME. Note: that is a STBT trigger happens while an ITBT is in progress, the ITBT is terminated and the STBT operation is initiated. If either of these is in operation a bit is set in a status register and VME is not allowed to read the TBT data.

The reading of the RMD is only allowed when the state machine is stopped, and this data is only available via the VME interface. This is the only data available to VME on this card. The VME Address lines 20:23 are compared with the 4-bit address switch to determine if the card is being addressed. VME Address lines

1:2 are channel select, VME address 0 is byte select (only used if reading in byte mode) and VME address lines 3:18 are the 64k RMD pointer. Note: the RMD is a 64k deep circular buffer used to store raw data, the time stamps for this data are stored on the TC.

Revised 5/24/04

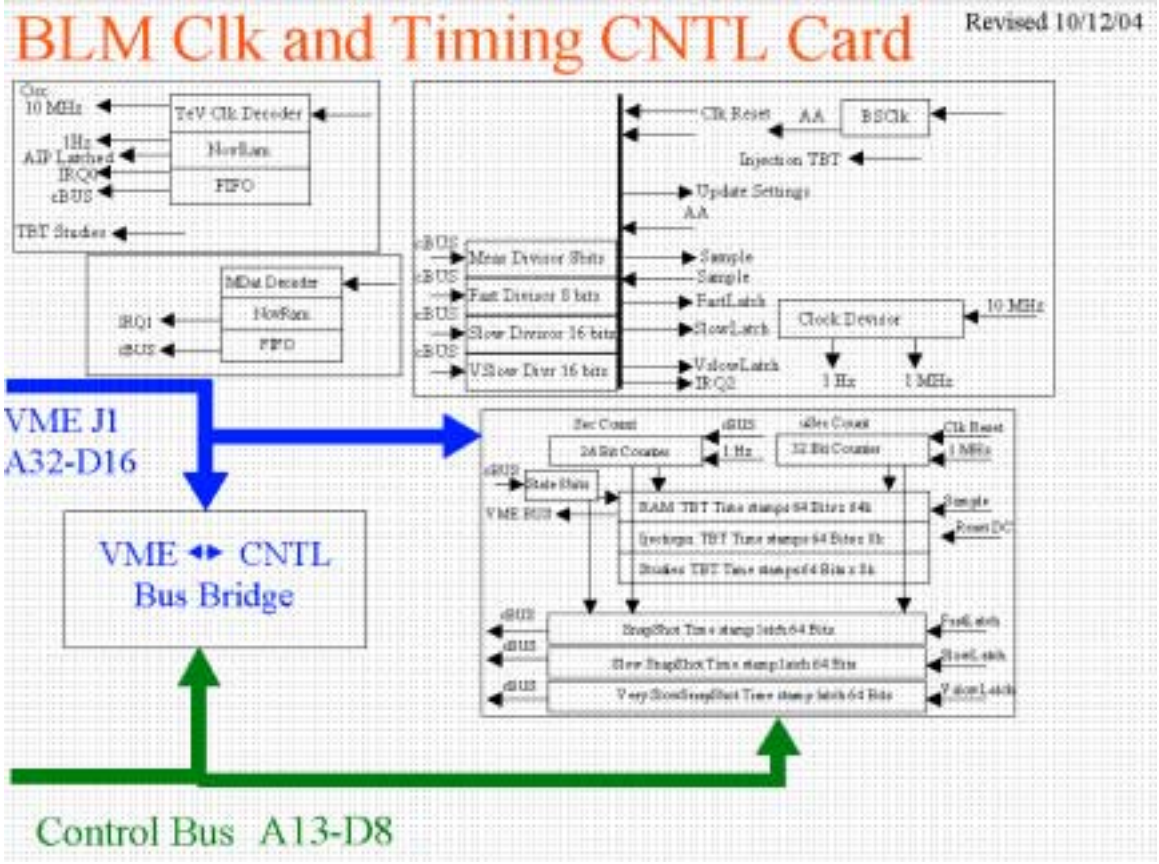
Digitizer Card FPGA Internal Registers
(Byte Count)[Bits] ~140 bytes

Channel 0		Address (A7-A0) 00-FF
4 [32]	Fast Sum Threshold R/W	00-03
4 [32]	Slow Sum Threshold R/W	04-07
4 [32]	Very Slow Sum Threshold R/W	08-0B
2 [16]	Imediate Threshold R/W	0C-0D
4 [32]	Fast Sum Latched R	10-13
4 [32]	Slow Sum Latched R	14-17
4 [32]	Very Slow Sum Latched R	18-1B
2 [16]	Mode select R/W	1C-1D
2 [16]	MADC Manual setting R/W	1E-1F
2 [16]	Current reading R	20-21
Channel 1		
4 [32]	Fast Sum Threshold R/W	30-33
4 [32]	Slow Sum Threshold R/W	34-37
4 [32]	Very Slow Sum Threshold R/W	38-3B
2 [16]	Imediate Threshold R/W	3C-3D
4 [32]	Fast Sum Latched R	40-43
4 [32]	Slow Sum Latched R	44-47
4 [32]	Very Slow Sum Latched R	48-4B
2 [16]	Mode select R/W	4C-4D
2 [16]	MADC Manual setting R/W	4E-4F
2 [16]	Current reading R	50-51
General		
2 [16]	Fast Sum Length R/W	F0-F1
2 [16]	Slow Sum Length R/W	F2-F3
2 [16]	Very Slow Sum Length R/W	F4-F5
2 [16]	TBT Ram Pointer R	F6-F7
2 [16]	FPGA Control Register R/W	F8-F9
2[16]	ADC Temperature	FC-FD
Channel 2		60-81
Channel 3		90-B1

IV) Timing Card

The timing card TC is the primary controller for data collection in the system, it has on board

1) Control Bus Interface for setting parameters
2) A TCLK decoder. This is used to receive the encoded TCLK events such as clkrst, and AIP. Receiving a TCLK event causes IRQ0 to be asserted. A 1 MHz clock is derived from this clock. In locations without a TCLK, an optional 10 MHz oscillator is provided.



3) A BSCLK decoder. This is used to receive the encoded BeeamSync Clk events such as AA. This AA marker is optionally used to make the Make_Meas signal. Note: the Make_Meas signal can also be derived by deviding the AA marker such as for Main Injector where Make_Meas is AA/2.
4) An MDAT decoder. This is used to receive machine state information from the MDAT system. Different machine states require different abort thresholds etc. Receiving an MDAT event causes IRQ1 to be asserted.
5) 512kbytes of RAM for storing 64k of Raw Measurements Data Time Stamps (RMDTS) these are stored as 8 Bits of State, 32 Bits unix time in seconds, and 24 bits of microseconds since last 1Hz clock event.
6) 128kbytes of RAM for storing TBT time stamps.
7) a VME interface only used for reading RMDTS an only accessible when system is stopped, and for reading TBT Time Stamps when TBT Not in operation.
8) A 8 bit switch selectable card number which sets VME addresses.
9) CA12=1, and CA8:11=Switch(0:3) are card select for control Bus.
10) A 24-bit microsecond counter reset by TCLK 1Hz event
11) A 32 bit Real Time Clock counting in seconds
12) An 8 bit devisor of the 1 MHz clock used to make the Make_Meas bus signal. The Make_Meas signal is generated by this divisor OR from the AA marker from BSClk, or from the AA Marker /2 for MI. The Make_Meas signal also latches the time stamp data 64 bits and writes it into the RMDTS ram array and increments the RAM Pointer. The Reset_DC signal zeroes this pointer.
13) An 8 bit devisor of the Make_meas signal used to make the Fast_Latch Signal

14) A 16 bit devisor of the Make_meas signal used to make the Slow_Latch Signal
15) A 16 bit devisor of the Make_meas signal used to make the Very_Slow_Latch Signal. Note all of these latch signals set a bit in a register and cause IRQ2 to be asserted so that the CC knows to go read the latched data. These 3 latch signals also latch the current time stamp into 3 registers so that the time stamp can also be read for each of these.
16) Writeable registers to force the creation of Reset_DC, AIP, Clear AIP etc
17) Front Panel lemo inputs which also make Reset_DC, AIP, and Clear AIP
18) The AIP signal being asserted causes the state machine to stop making all control pulses, Make_meas, xxxx_latch, etc. effectively freezing all buffers in the system. AIP is a latched signal cleared by Clear_AIP and by RESET.
19) ITBT Trigger. This line is driven onto the backplane in response to a BSCLK Injection clock event, it causes the 8k Injection TBT buffer to be filled on the digitizer cards as well as the injection TBT time stamps to be filled on the TC.
20) STBT Trigger. This line is driven onto the backplane in response to a TCLK Studies clock event, it causes the 8k Studies TBT buffer to be filled on the digitizer cards as well as the Studies TBT time stamps to be filled on the TC.

[AEB1]The Timing Card is controlled by signals on the control bus and by TCLK, BSCLK, and MDAT events. These signals are:

1) Reset, Reset. This signal is the BLM Crate reset signal, driven by the Controller Card (CC) it should reset the state machine on the TC.
2) Reset_DC, Reset Digitizer Card. This signal clears the sliding sums and resets the RMDTS pointer to 0000. This signal typically is used to initialize the TC and get ready for data taking.
3) Make_meas, Make Measurement. This signal is generated on the Timing Card (TC) and typically runs continuously at about once every 20 microseconds. On the TC this signal causes a time stamp to be placed into the RDMTS Ram circular buffer.
4) Fast_Latch, This is a signal produced on the TC which tells the state machine to latch the current Fast_Sum Time Stamp into a register so the controller can read it
5) Slow_Latch, This is a signal produced on the TC which tells the state machine to latch the current Slow_Sum Time Stamp into a register so the controller can read it
6) VSlow_Latch, This is a signal produced on the TC that tells the state machine to latch the current Very_Slow_Sum Time Stamp into a register so the controller can read it. Each of these latch signals also sets a bit in a register and causes the TC to assert the IRQ2 line so that the CC knows to fetch data into its larger circular buffers.
7) CA(0:12), Control Bus Address lines. These are used to address control and data within the state machine. These are driven by the CC.
8) Cdata(0:7) Control Bus Data Lines. These are the data lines used to read and write data to and from the state machine.
9) MemRD*, Memory read. This indicates that the current Control Bus cycle is a read.
10) MemWR*, Memory write. This indicates that the current Control Bus cycle is a write.
11) WE*, Memory Write Enable. This is the write strobe for data, data should be latches on the rising edge of WE*

Timing Card FPGA Internal Registers (Byte Count)[Bits] ~64 bytes

Revised 10/13/04

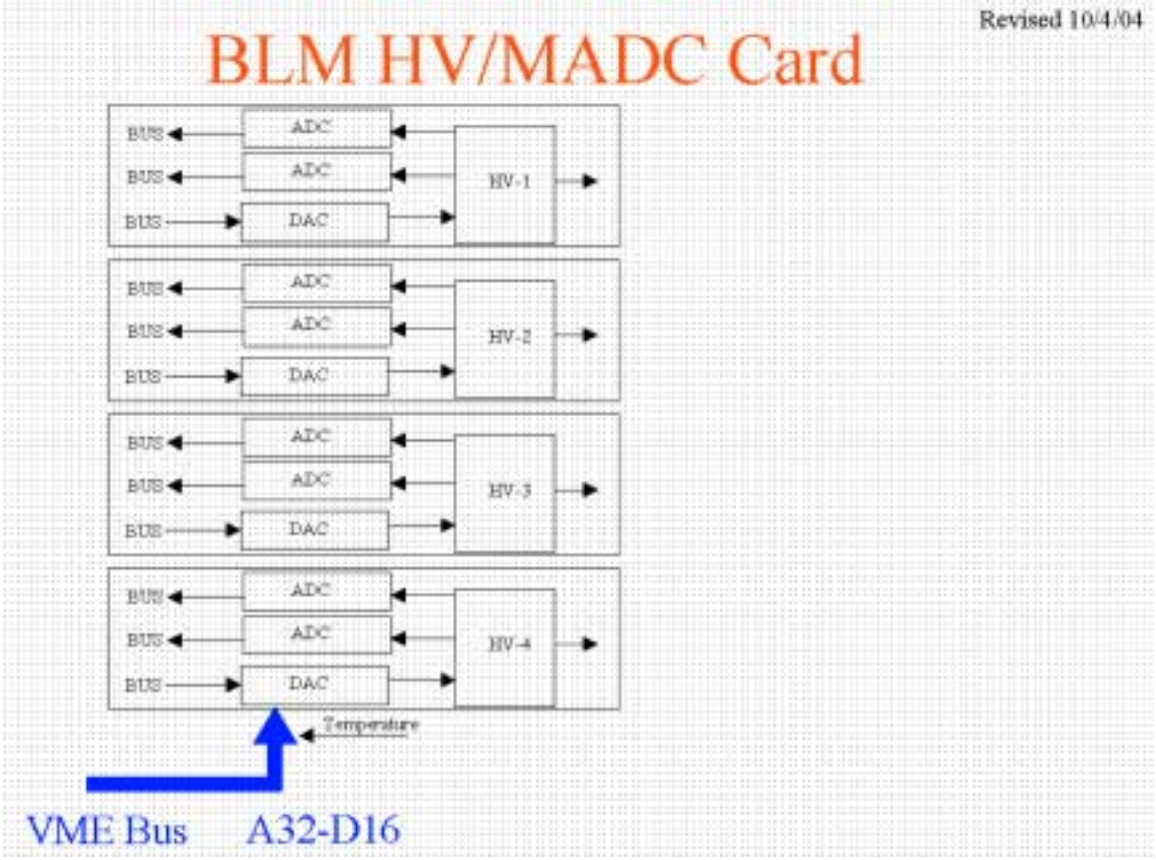
Setup		Address (A7:A0) 00:FF
2 [16]	CSR R/W	00-01
1 [8]	State Number R/W	02
1 [8]	Status R	03
4 [32]	Seconds Time Clock setting W	04-07
1 [0]	Set Clock on next (8F)	08
1 [0]	Update Settings on next Make_Meas	09
2 [16]	MDAT Frame ID R/W	0A-0B
1 [8]	TCLK or BSCLK Number R/W	0C
1 [8]	TCLK Prom Setting W	0D
1 [8]	BSClk Prom Setting W	0E
Controller		
1 [8]	Make Meas Divisor R/W	10
1 [8]	Imediate Sum Length	11
1 [8]	Fast Sample Length R/W	12
2 [16]	Slow Sample Length R/W	14-15
2 [16]	Very Slow Sample Length R/W	16-17
2 [16]	TBT Ram Pointer R	20-21
1[8]	TCLK Event FIFO R	30
1[8]	BSCLK Event FIFO R	31
2 [16]	MDAT Event FIFO R	32-33
Clocks/Timing		
8 [64]	Fast Latch Time Stamp R	40-47
8 [64]	Slow Latch Time Stamp R	48-4F
8 [64]	Very Slow Latch Time Stamp R	50-57
General		
1 [0]	Force Clear W	F0
1 [0]	Force Start (Reset DC) W	F1
1 [0]	Force Stop W	F2
1 [0]	Force ClkReset (8F) W	F3
1 [0]	Force AIP W	F4
1 [0]	Force Sum Latches	F5
1 [0]	Force ITBT Trigger	F6
1 [0]	Force STBT Trigger	F7
3 [3]	IRQ2 Status Reg R W=Clr	F8-FA
Diagnostics		
2[16]	ADC Temperature	FE-FF

The reading of the RMDTS is only allowed when the state machine is stopped, and this data is only available via the VME interface. This is the only data available to VME on this card. The VME Address lines 24:31 are compared with the 8 bit address switch to determine if the card is being addressed. VME A20:23=0000, VME Address line 19 =0 is used to indicate that the RMDTS is being accessed. VME Address lines 1:2 are time stamp word select, VME address 0 is byte select (only used if reading in byte mode) and VME address lines 3:18 are the 64k RMDTS pointer. Note: the RMDTS is a 64k deep circular buffer used to store raw data time stamps. VME A19=1, is the dual TBT Buffers and Register space on the TC.

The TC also includes a VME to Control Bus Bridge to allow for setting up the DC and TC hardware in situations where a CC module is not present. The VME Address lines 24:31 are compared with the 8 bit address switch to determine if the card is being addressed. A20:23=0001, VME Address line 20 =1

is used to indicate that the Bridge is being accessed. If the bridge is being accessed then VME Addresses 1:13 are copied to Control addresses 0:12 and control bus data lines 0:7 are connected to VME data lines 0:7. The bridge must also use appropriate VME signals to create the following Control Bus signals: MEMRD*, MEMWR*, and WE*. The TC will pull Bus line CPU_Detect High, if this line is sensed low the bridge will be Disabled since there is a CC present.

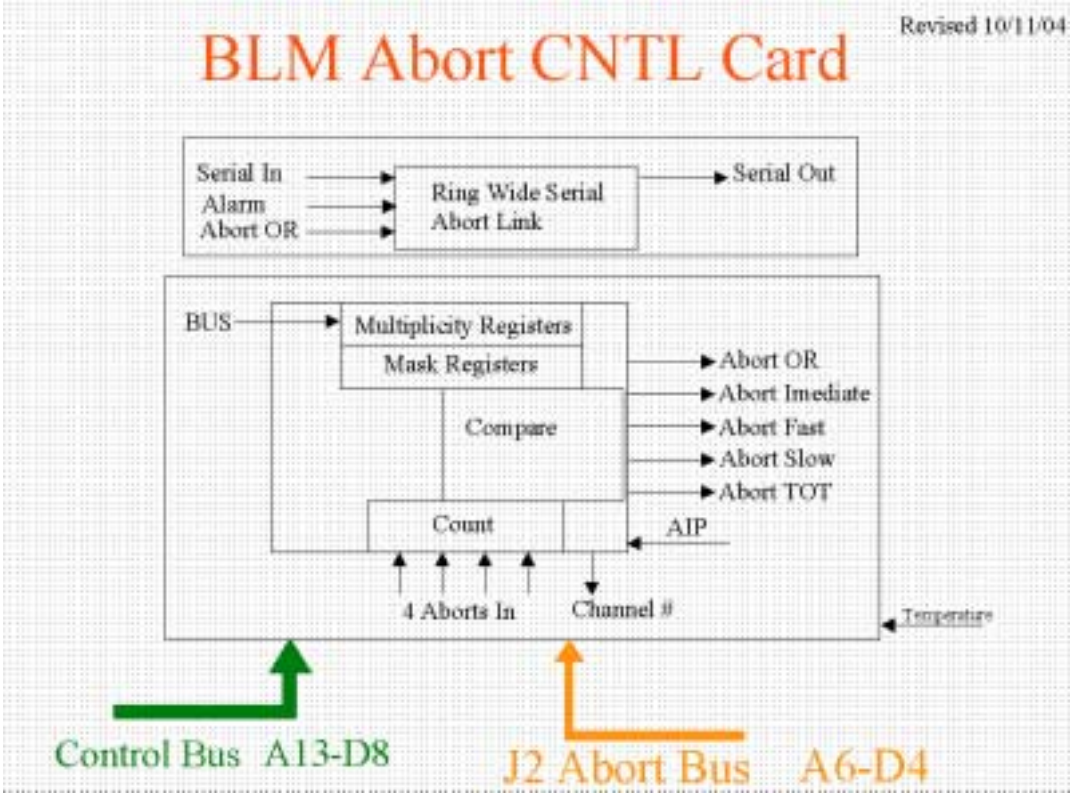
V) HV Card



The High Voltage Card HVC is the primary HV power supplier for the loss monitor tubes, it has on board

1) VME Interface for setting and reading parameters
2) A 8 bit switch selectable card number which sets VME address 24:31 addresses.
3) 1 or 4 HV Power Supplies (DC-DC converters) controlled by
4) 1 or 4 16 bit Digital to Analog Converter 0-10V
5) 2 16-bit ADCs for reading back the HV out and HV return. If there are 4 supplies then there would be 8 ADCs
6) Note: the HV supplies are good for about 30 microAmps. So the Resistive divider used to down convert the 3000V to 10 V will have to be made from very large (gigaOhm) resisters, even a 1 GOhm would draw 3 microAmps so that reading both the output and the return would use 6 of the 30 microAmps available. My guess is that we will need 10Gohm.
7) THIS CARD DOES NOT TALK Control Bus!!

VI) Abort Controller Card



The Abort Controller Card ACC is the primary controller for abort collection and reporting, it has on board

1) Control Bus Interface for setting parameters

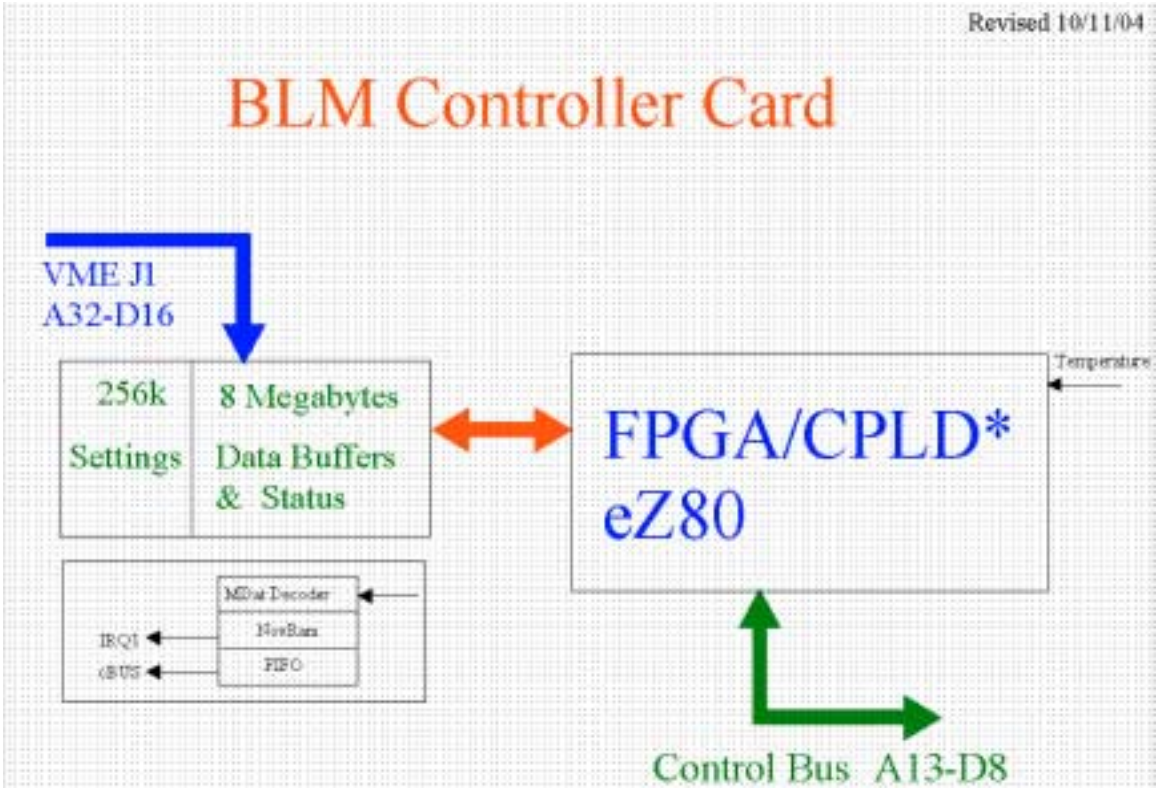
Revised 10/13/04

ACC Card FPGA Internal Registers
(Byte Count)[Bits] ~32 bytes

Masks		**Address (A7-A0) 00-FF**
1 [6]	Abort Mask R/W	00
1 [6]	Abort Channel Count	01
8 [64]	Imediate Abort Masks R/W	10-17
8 [64]	Fast Abort Masks R/W	18-1F
8 [64]	Slow Abort Masks R/W	20-27
8 [64]	Very Slow Abort Masks R/W	28-2F
8 [64]	New Abort Masks R/W	30-37
Multiplicities		
1 [6]	Imediate Multiplicity R/W	40
1 [6]	Fast Multiplicity R/W	41
1 [6]	Slow Multiplicity R/W	42
1 [6]	Very Slow Multiplicity R/W	43
1 [6]	New Multiplicity R/W	44
General		
1[6]	Force Abort H R/W	45
1[6]	Force Abort L R/W	A4
1[6]	Force Abort Permit R/W	A5
Diagnostic		
2[16]	ADC Reading Temperature	4E-4F

2) A 4 bit switch selectable card number which sets Control Bus addresses. CA12=1, and CA8:11=Switch(0:3) are card select for control Bus.
3) A state Machine which upon receipt of a Make_Meas signal, cycles through all 64 possible channel numbers, puts Abort_CS(0:5) out on the bus and reads the results back on Abort(0:3). For each of the abort types, this state machine counts the number of channels that are requesting an abort AND which are not masked OFF. Once it has read all channels, it does a comparison of the number for each abort type against the abort type's Multiplicity number. If the count is greater than the multiplicity then that abort line is asserted. The "OR" of all 4 abort types is also asserted.
4) This Card will have an additional Serial Data Link that will allow for the ring-wide abort data to be collected.
5) THIS CARD DOES NOT TALK VME!!

VII) Controller Card



The Controller Card CC is the primary controller for the Tevatron BLM system. It Has on board:

1) Control Bus Interface Master for setting parameters and reading back sliding sums, etc.
2) A 8 Megabyte Block of shared memory with the VME bus, this is used for getting setup parameters and for storing the circular buffers and other frame memories.
3) An MDAT decoder. This is used to receive machine state information from the MDAT system. Different machine states require different abort thresholds etc. Receiving an MDAT event causes IRQ1 to be asserted. This is an option for the CC.
4) An 8 bit switch selectable card number which sets VME address 24:31 addresses. Shared memory is then from 000000-7FFFFE (A1:23)
5) Interrupt control lines IRQ(0:3) which alert the controller that hardware need servicing.

6) CA(0:12), Control Bus Address lines. These are used to address control and data within the state machine. These are driven by the CC.
7) Cdata(0:7) Control Bus Data Lines. These are the data lines used to read and write data to and from the state machine.
8) MemRD*, Memory read. This indicates that the current Control Bus cycle is a read.
9) MemWR*, Memory write. This indicates that the current Control Bus cycle is a write.
10) WE*, Memory Write Enable. This is the write strobe for data, data should be latches on the rising edge of WE*
11) The CC will drive Bus Control line CPU_detect Low to cause The VME to Control Bus Bridge on the TC to be disabled. This is required since the control bus is a single master bus.
12) 2 RS-232 ports for diagnostics and standalone operation

13) A TCP/IP 10/100 baseT port for standalone operation. MOOC/ACNET NOT! Supported.

Revised 10/11/04

Controller Card VME Memory Map

8192k Address space A32-D16

256 State Settings Buffer	256k		256 State Settings Buffer	256k
256 State Settings Buffer Copy	256k		256 State Settings Buffer Copy	256k
512 Monitor Buffer (Temp,V etc)	1k		512 Monitor Buffer (Temp,V etc)	1k
512 Control Buffer (MADC,HV etc)	1k		512 Control Buffer (MADC,HV etc)	1k
16 Pointers Buffer	1k	OR	16 Pointers Buffer	1k
1*3 Display Buffer	1k		1*3 Display Buffer	1k
2*128*3 Profile Buffer	210k		2*128*3 Profile Buffer	210k
128*3 Flash Buffer	105k		128*3 Flash Buffer	105k
4K Very Slow Snapshot Memory	1106k		4K Very Slow Snapshot Memory	1106k
4K Slow Snapshot Memory	1106k		4K Slow Snapshot Memory	1106k
8K Snapshot Memory	2212k		16K Snapshot Memory	4424k
Total 5149k (reserved) 8MB			Total 7361k (reserved) 8MB	
000000-7FFFFF			000000-7FFFFF	

Revised 10/5/04

BLM eZ80 Memory Allocation

Function	Size	Address Range	
Control Bus	8 kB	6x0000-6x1FFF Upper 4 Address Decoder 0110	BLM Control Bus
10/100 BaseT	1 MB	500000-5FFFFF Upper 4 Address Decoder 0101	10/100 BaseT
MDAT	1k	6x2000-6x20FF Upper 4 Address Decoder 0101	10/100 BaseT
VME Dual Port	8 MB	800000-FFFFFF Upper 4 Address Decoder 1xxx	VME to FPGA/CPLD Dual Port
CPU RAM	2 MB	200000-3FFFFF Upper 4 Address Decoder 001x	CPU RAM Memory
Program Memory	2 MB	000000-1FFFFF Upper 4 Address Decoder 000x	Program Memory

VME Addressing

Revised 10/5/04

BLM VME Memory Allocation Example

Switch Settings			Address Range
0000	Digitizer Card(0)	1 MB	000000-0FFFFF
0001	Digitizer Card(1)	1 MB	100000-1FFFFF
0010	Digitizer Card(2)	1 MB	200000-2FFFFF
0011	Digitizer Card(3)	1 MB	300000-3FFFFF
0100	Digitizer Card(4)	1 MB	400000-4FFFFF
0101	Digitizer Card(5)	1 MB	500000-5FFFFF
0110	Digitizer Card(6)	1 MB	600000-6FFFFF
0111	Digitizer Card(7)	1 MB	700000-7FFFFF
1000	Digitizer Card(8)	1 MB	800000-8FFFFF
1001	Digitizer Card(9)	1 MB	900000-9FFFFF
1010	Digitizer Card(A)	1 MB	A00000-AFFFFF
1011	Digitizer Card(B)	1 MB	B00000-BFFFFF
1100	Digitizer Card(C)	1 MB	C00000-CFFFFF
1101	Digitizer Card(D)	1 MB	D00000-DFFFFF
1110	Digitizer Card(E)	1 MB	E00000-EFFFFF
1111	Digitizer Card(F)	1 MB	F00000-FFFFFF
A32-D16			
00000001	Timing/Bridge Card	2 MB	XXXXXX
A32-D16			
00000010	High Voltage Card	1 MB	XXXXXX
A32-D16			
00000011	Controller Card	8 MB	XXXXXX

Digitizer Card Memory xX00000H - xXFFFFFH
Digitizer Card Memory xX00000H - xXFFFFFH
•
•
•
•
•
•
•
Digitizer Card Memory xX00000H - xXFFFFFH
Digitizer Card Memory xX00000H - xXFFFFFH

Revised 10/5/04

BLM Digitizer Card VME Memory Map

1024k Address space

VME Access A24

A23-A20 = Switch Setting
Then: IF A19=0 main turns memory 64k turns
A2,A1 = CHANNEL 0/1/2/3
A18-A3 = Turns number which wraps at 64k(Decrements FFFF-0000)
A18-A1 = 00000-7FFFE = 512KB of TBT Data (64k Turns)
Readable only when Stopped
If A19=1 then
A18-A1 = 00000-0FFFE = 64KB of TBT Data (8k Turns) Injection(Increments)
A18-A1 = 10000-1FFFE = 64KB of TBT Data (8k Turns) Studies(Increments)
Readable only when Stopped or NOT doing turn studies

A18-A1 = 7E000-7FFFE = 8KB of Settings, ID etc

Revised 10/5/04

BLM Timing Card VME Memory Map

2048k Address space

VME Access A32

A31-A24 = Switch Setting 8 Bits (default 00000001)

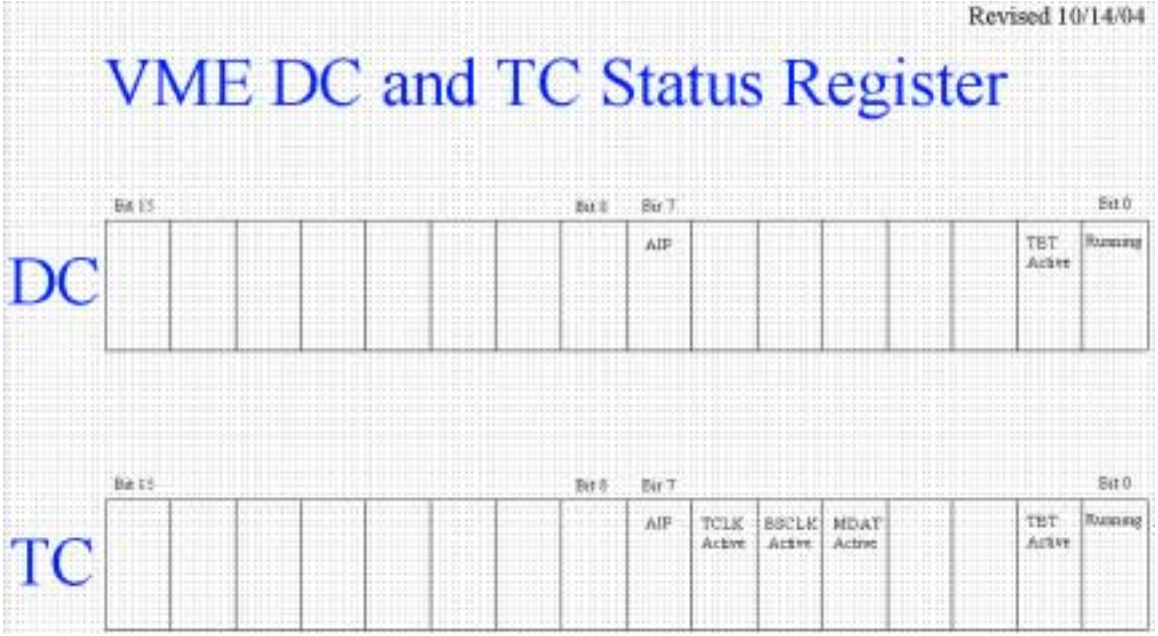
A23-A21 = 000

IF A20=0 then

Then: IF A19=0 main turns memory 64k turns
A2,A1 = Time Stamp Words 0/1/2/3
A18-A3 = Turns number which wraps at 64k(Decrements FFFF-0000)
A18-A1 = 00000-7FFFE = 512KB of TBT Data (64k Turns)
Readable only when Stopped
If A19=1 then
A18-A1 = 00000-0FFFE = 64KB of TBT Data (8k Turns) Injection(Increments)
A18-A1 = 10000-1FFFE = 64KB of TBT Data (8k Turns) Studies(Increments)
Readable only when Stopped or NOT doing turn studies
A18-A1 = 7E000-7FFFE = 8KB of Settings, ID etc

If A20=1 then VME to CNTL Buss Bridge

VME A13-A1 = CNTL A12-A0 and A19-A14 are don't care



BLM VME Memory Map

BLM Digitizer Card Memory Map (1 MB)

BLM digitizer cards respond to A24D16 and may take all of the A24D16 address space (16 MB) since there may be up to 16 digitizer cards.

Each Card's address is A24-D16 (N00000-NFFFFE) where N is card number 0-F
A23-A20 = Switch Setting 0-F

Then: IF A19=0 main turns memory 64k turns
A2,A1 = CHANNEL 0/1/2/3
A18-A3 = Turns number which wraps at 64k(Decrements FFFF-0000)
A18-A1 = 00000-7FFFE = 512KB of TBT Data (64k Turns)

VIII) Readable only when Stopped

If A19=1 then
A18-A1 = 00000-0FFFE = 64KB of TBT Data (8k Turns)
Injection(Increments)
A18-A1 = 10000-1FFFE = 64KB of TBT Data (8k Turns)
Studies(Increments)
Readable only when Stopped or NOT! doing turn studies

A18-A1 = 7E000-7FFFE = 8KB of Settings, ID etc

BLM Timing Card Memory Map (2 MB)
A32-D16 (02000000-021FFFFE)
A31-A24 = Switch Setting 8 Bits (default 00000010)

A23-A21 = 000

IX) IF A20=0 then
Then: IF A19=0 main turns memory 64k turns
A2,A1 = Time Stamp Words 0/1/2/3
A18-A3 = Turns number which wraps at 64k(Decrements FFFF-0000)
A18-A1 = 00000-7FFFE = 512KB of TBT Data (64k Turns)
Readable only when Stopped
If A19=1 then
A18-A1 = 00000-0FFFE = 64KB of TBT Data (8k Turns) Injection (Increments)
A18-A1 = 10000-1FFFE = 64KB of TBT Data (8k Turns) Studies (Increments)
Readable only when Stopped or NOT! doing turn studies
A18-A1 = 7E000-7FFFE = 8KB of Settings, ID etc

If A20=1 then VME to CNTL Buss Bridge
VME A13-A1 = CNTL A12-A0 and A19-A14 are don't care

BLM High Voltage Card Memory Map (1 MB)
A32-D16 (03000000-030FFFFE)

BLM Controller Card Memory Map (8 MB)

The controller card has the shared memory in the system, and thus contains all settings and parameters as well as the large circular buffers.
X) A24-31=switch setting, default = 00000001
A32-D16 (01000000-017FFFFE)
All addresses are added to card base address.

000000 Status

000012 Time Setting Status
000014 Time Setting 16 MSb

000016 Time Setting 16 LSb

Settings General:
000100 Channel Count
000102 Immediate Sum Length
000104 Fast Sum Length
000106 Slow Sum Length
000108 Very Slow Sum Length
00010A Digitizer Control Settings 1
00010C Digitizer Control Settings 2
00010E Timing Card Control Settings 1
000110 Timing Card Control Settings 2

000200 Channel 0 MADC Control
000202 Channel 0 MADC Setting
.
.
0002FC Channel 63 MADC Control
0002FE Channel 63 MADC Setting

000300 Channel 0 Mode Control
000302 Channel 1 Mode Control
.
.
00037E Channel 63 Mode Control

Abort Machine States (256) are in the following Block:

State Type 0: (001000-0013FE)

001000 State Number, Action Marker 0=NOP
001002 Channel Masks 0 1 for Immediate Abort
001004 Channel Masks 2 3 for Immediate Abort
001006 Channel Masks 4 5 for Immediate Abort
001008 Channel Masks 6 7 for Immediate Abort
00100A Channel Masks 0 1 for Fast Abort
00100C Channel Masks 2 3 for Fast Abort
00100E Channel Masks 4 5 for Fast Abort
001010 Channel Masks 6 7 for Fast Abort
001012 Channel Masks 0 1 for Slow Abort
001014 Channel Masks 2 3 for Slow Abort
001016 Channel Masks 4 5 for Slow Abort
001018 Channel Masks 6 7 for Slow Abort
00101A Channel Masks 0 1 for Very Slow Abort

00101C Channel Masks 2 3 for Very Slow Abort
00101E Channel Masks 4 5 for Very Slow Abort
001020 Channel Masks 6 7 for Very Slow Abort
001022 Abort Multiplicity for Immediate and Fast Abort
001024 Abort Multiplicity for Slow and Very Slow Abort

001026-00102E Spares

001030 Channel 0 Immediate Threshold LSBs
001032 Channel 1 Immediate Threshold LSBs
.
.
0010AE Channel 63 Immediate Threshold MSBs

0010B0 Channel 0 Fast Threshold LSBs
0010B2 Channel 0 Fast Threshold MSBs
0010B4 Channel 1 Fast Threshold LSBs
0010B6 Channel 1 Fast Threshold MSBs
.
.
0011AC Channel 63 Fast Threshold LSBs
0011AE Channel 63 Fast Threshold MSBs

0011B0 Channel 0 Slow Threshold LSBs
0011B2 Channel 0 Slow Threshold MSBs
0011B4 Channel 1 Slow Threshold LSBs
0011B6 Channel 1 Slow Threshold MSBs
.
.
0012AC Channel 63 Slow Threshold LSBs
0012AE Channel 63 Slow Threshold MSBs

0012B0 Channel 0 Very Slow Threshold LSBs
0012B2 Channel 0 Very Slow Threshold MSBs
0012B4 Channel 1 Very Slow Threshold LSBs
0012B6 Channel 1 Very Slow Threshold MSBs
.
.
0013AC Channel 63 Very Slow Threshold LSBs
0013AE Channel 63 Very Slow Threshold MSBs

0013B0-0013FE Spares

Then the rest are the same as state 0

001400-0017FE State 1 settings
001800-001FFE State 2 settings
.
.
03F800-03FFFE State 255 Settings

040100-07FFFE Copy of settings that are in use

BLM Display Frames

080000-08010C BLM Display Frame Fast
08010E-08021A BLM Display Frame Slow
08021C-080329 BLM Display Frame Very Slow

XI) BLM Flash Frames

080350 BLM Flash Frame Counter
080352-08045E Flash Frame 0
080460-08046C Flash Frame 1
.
.
.
088946-088A52 Flash Frame 127

XII) BLM Profile Frames

088A60 BLM Profile Frame Counter
088A62-088B6E Profile Frame 0 Fast
088B70-088C7C Profile Frame 0 Slow
088C7E-088D8A Profile Frame 0 Very Slow
088D8C-088E98 Profile Frame 1 Fast
.
.
.
0A1E54-0A1F62 Profile Frame 127 Very Slow

Circular Buffers:
Each circular buffer is made from BLM frames each being 270 bytes in length (10E)

Fast Snapshot buffer (16K)

0A1FF0 – 0A1FF2 Snap Pointer (24 bits) Points to most recent frame.

0A2000-4D9FFE (16k * 270) Circular Buffer

Slow Snapshot Buffer (4K)

4DA0FC-4DA0FE Snap pointer (24 bits) Points to most recent frame.

4DA100-5E80FE (4k * 270) Circular Buffer

Very Slow Snapshot Buffer (4K)

5E81FC-5E81FE Snap pointer (24 bits) Points to most recent frame.

5E8200-6F61FE (4k * 270) Circular Buffer

Channel Pedestal Storage (64 channels x 16 bits)
6F6200-6F627E

6F6300-7FFFFE Future expansion~ 1 MB

NEW BLM Data Structures

Each BLM data entry (FastSnapShot, SlowSnapshot, VerySlowSnapshot, Flash, Profile, and Display) has (256) bytes defined as follows:

(240 bytes containing the 60 Loss Monitor's Sliding Sum data)

1 State Byte
    Has BLM Machine state 0-255

1 Byte Measurement Divisor
2 Bytes Sum Divisor
1 Abort Status Byte
    Status Bit 0 = Abort 0
    Status Bit 1 = Abort 1
    Status Bit 2 = Abort 2
    Status Bit 3 = Abort 3
    Status Bit 4 = NC
    Status Bit 5 = NC
    Status Bit 6 = NC
    Status Bit 7 = NC
1 Byte Channel Count
7 Bytes Time Stamp
    4 Bytes of Seconds
    3 Bytes of MicroSeconds since last 1 Hz Event
(3) Byte Spare

BLM Operational Description

The new BLM system is designed to do several tasks, first is to provide a flexible and reliable abort system to protect Tevatron magnets, second is to provide loss monitor data during normal operations, and lastly to provide detailed diagnostic loss histories when an abort happens.

The new BLM system resides in a Standard VME format crate with a standard J1 backplane and a custom J2 backplane for the BLM Busses. The system communicates with the outside world via ACNET through a standard VME host CPU. This VME host sets the parameters in the BLM system trough a block of shared memory in the BLM CPU (a Zilog eZ80, 24 bit address, 8 bit data, 50 MHz microcontroller.)

The BLM system has essentially 3 busses, a VME bus, The BLM Control bus J2-A row, and the Abort Bus J2-C row. All operations on the Abort bus are done from the ACC via its state machine. All operations on the Control bus are done from the CC via eZ80 software. VME can access the control bus only in systems without a CC, via a VME to Control bus bridge on the TC. Normally the VME places data into the shared memory on the CC, and the CC puts that data into the hardware.

All hardware parameters are set from the CC over the dedicated BLM control bus. This control bus has 13 address lines(CA12:0) and 8 data lines(CD7:0). The addressing of this bus is as follows:

1) If CA(12)=0 then the control bus is talking to a digitizer card whose switch setting is equal to CA(11:8).
2) If CA(12)=1 and CA(11:8) =0000 then the control bus is talking to the Timing Card
3) If CA(12)=1 and CA(11:8)=0001 then the control bus is talking to the Abort concentrator card.

Note: the same 4 switches set the high 4 bits of the DC's VME address (A23:20) and the high 4 bits of the AbortCS lines

Each card has 256 bytes of address space (CA(7:0)) which makes up its memory register space. This register space is defined elsewhere. The BLM CPU has a setup table for each of a possible 256 machine states, and will load this data into the hardware in response to an MDAT state change. These settings only effect the Digitizer Cards and the Abort concentrator card. The settings for the Timing card do not change with machine state, and should only be changed during beam off periods.

An important feature of the BLM system is that all abort operations are handled by state machines, once setup by the CC, these operations proceed without intervention from either VME or eZ80. The only things that the CPUs do is setup the parameters.

In order to smoothly update the new settings in the DCs and ACC, these cards must double buffer all registers with the first register being written via the BLM Control bus. The data is transferred to the actual usage register via a backplane signal "Update Settings" which will occur after all settings have been written and will be synchronous with the "Make_Meas" signal. This "Update Settings" signal is generated on the timing card so as to be sync'd with the Make_meas and is generated in response to a command from the CC.

BLM Normal Operational

Once the settings are loaded into the TC, DCs and ACC, the system is ready to run. The BLM operations are initiated by a clock event such as “Prepare for Beam” which will cause the TC to issue a Digitizer Card Reset, DC_Reset, on the control bus. The DC_Reset causes the DCs to zero all sliding sums and causes the DCs and the TC to set all buffer pointers to 0000. This assures that all buffers are synchronized and ready to take data.

The primary clock for the BLM system, Make_Meas, is derived from the AA marker on the beam sync clock (Typically 21 uSec). Make_Meas is transmitted on the BLM control bus to all BLM cards. Optionally the Make_Meas signal can be created by dividing the AA marker, or by dividing down an internal clock. The shortest allowable period for this signal is 12 microseconds due to the reset time needed by the integrators.

On the digitizer cards the Make_Meas signal causes the DC to latch the abort request states for each channel and for each sliding sum from the previous sample period. It also defines the sample period so that the Make_Meas signal causes the integrators to switch from integrator A to B or B to A, and triggers the ADCs to convert which in turn causes the sliding sums to be updated and all abort comparisons to be made. At this time the new ADC readings are written to a 64k deep circular buffer which is used for diagnostic purposes as well as the source of the sliding sums. The new ADC Data may also be written to 1 of 2 TBT dedicated studies buffers. The abort states are latched on the next Make_Meas. Thus the DC has the full sample period to do it’s conversions, make the sliding sums and do the abort compare with thresholds.

On the ACC the Make_Meas signal causes the abort summing state machine to cycle through each BLM channel by putting the channel address, ACS(5:0) out on the abort bus on the BLM control Bus and to read back from each channel the state of each of its abort requests ABORT(3:0). For each abort type, each channel has an abort mask bit which determines if that channel is allowed to request an abort of that type. A count is made for each of the 4 abort types of allowed AND requesting channels which are above threshold. If the sum of channels requesting an abort for any of the 4 abort types equals or exceeds the abort multiplicity setting for that abort type, an abort request is transmitted off card on a 50 ohm TTL line driver.

This Make_Meas signal, therefore causes the data to be taken and the abort logic to be updated every cycle. (21 uSec). So that even though a sliding sum might be the sum over 500 samples (10 mSec) it’s abort threshold is compared every 21 uSec. This completes the description of the Abort logic part of the operation.

The DCs also make and update every 21uSec, 3 sliding sums of samples. These sliding sums are compared every cycle to their abort limits. However, for diagnostic purposes, these sums are stored periodically in circular buffers on the CC. This process is controlled by the TC, which periodically generates 3 latch signals, one for each sliding sum. The latch signals cause the DCs to latch the appropriate sum and the TC to latch the time stamp and to interrupt the CC so that it knows the data is latched and ready to be read and stored in the appropriate circular buffer.

Note: the individual ADC readings are 16 bits, however the sliding sums are 32 bit numbers. Therefore the dynamic range of, for example, the 1 second sliding sum is almost 32 bits. These sliding sums are the total integrated loss over the sum interval, not just samples of losses spaced in time.

At any given time, the BLM has a variety of stored loss histories with different time resolutions. The 64k raw measurement data provides 1.4 seconds of loss data with 21 uSec resolution. The 8k Circular buffer provides 8 seconds of integrated loss data with 1 ms resolution. The 4k slow circular buffer provides 200 seconds of integrated loss data with 50 mSec resolution. And the 4k Very slow buffer provides 4000 seconds, over an hour, of integrated loss data with 1 second resolution. As one can see, in the event of an abort, there is a very detailed history of losses prior to the abort, which may be examined to aid in diagnosing the problem.

BLM Special Diagnostic Buffers TBT

In addition to the diagnostic buffers mentioned above, which are circular buffers that are periodically overwritten, the BLM system has 2 linear buffers that are triggered and are not automatically overwritten. These 2 buffers are Turn-By-Turn (TBT) and are each 8k deep. The TBT Buffers are designed to match the capability of the new BPM system and allow the simultaneous sampling of beam position in the BPM and beam losses in the BLM.

The injection TBT buffer (ITBT) is designed to match the BPM injection TBT buffer and is triggered by ITBT_Trig at injection. The studies TBT buffer is designed to match the BPM TBT buffer used for beam studies. The STBT is triggered by STBT_Trig, both of these triggers are generated on the TC by clock events on TCLK or BSCLK. When either of these TBT buffers are triggered, the DCs and TC will set a bit in a status register indicating the TBT operations are in progress and that the TBT memory is not accessible from VME. Once the TBT operation completes, or if an abort happens, the DCs and TC will reset the status bit, and VME will have access to the TBT memory.

TBT operations will require the DCs and TC to not only write the large 64k circular buffer each sample period, but to also write the data into the TBT buffer each sample period.

The ITBT buffer once triggered, will fill to its limit of 8k and stop. It will not be overwritten until another injection clock event happens. If another ITBT_Trig happens, prior to the completion of the ITBT operation, the ITBT pointer will be reset to 0 and 8k of new TBT data will be written into the ITBT buffer.

The STBT buffer once triggered, will fill to its limit of 8k and stop. It will not be overwritten until another Studies clock event happens. If another STBT_Trig happens, prior to the completion of the STBT operation, the STBT pointer will be reset to 0 and 8k of TBT data will be written into the STBT buffer.

If a STBT_Trig happens during an ITBT operation, the ITBT operation is ended and the STBT pointer is set to 0 and an STBT operation is started. Thus only a single TBT operation is allowed at any given time. If this happens the host should be able to fully reconstruct the ITBT data using the ITBT and STBT buffers and their time stamps.

It also possible to provide a software TBT_Trig permit for each type of TBT buffer, so that the buffer could be “locked” and not overwritten unless it is “un-locked”.

Revision History:

1.00.00 First Posting in Doc DB. Date: 10/14/04